COMPUTER ARCHITECTURE (M.Tech. Optional Core)

Course Syllabus

July 2014

Credits: 3

Prerequisites: Computer Organization, Basics of Computer Architecture, Operating Systems.

UNIT - I: Fundamentals of Computer Design

Technology Trends, Measuring and Reporting Performance, Quantitative Principles of Computer Design, Power consumption and efficiency as the metric.

UNIT - II: Instruction Set Principles

Classifying Instruction Set Architectures, Memory Addressing, Addressing modes, Operations in the instruction set, Instructions for control flow, encoding an instruction set, interrupt processing, processor support for multiprogramming and threads.

UNIT - III: Instruction-Level Parallelism and its Dynamic Exploitation

Instruction level parallelism: concepts and challenges, overcoming data hazards with dynamic scheduling, dynamic scheduling algorithm, reducing branch costs with dynamic hardware prediction, high performance instruction delivery, thread level parallelism, branch prediction, VLIW approach, hardware support for exposing more parallelism at compile-time, pipelining

UNIT - IV: Memory Hierarchy Design

Memory hierarchy design, Review of ABCs of Caches, Cache performance, reducing cache miss penalty, reducing miss rate, reducing cache miss penalty and miss rate with parallelism, reducing hit time, main memory organizations and improving performance, virtual memory, protection of virtual memory.

UNIT - V: Multiprocessors and Thread-Level Parallelism

Symmetric shared-memory architectures and their performance, distributed shared-memory architectures and their performance, synchronization, models of memory consistency, multithreading: exploiting thread-level parallelism within a processor.

UNIT - VI: Storage Systems

Types of storage devices, Buses: connecting I/O devices to CPU/Memory, Reliability, Availability and Dependability, RAID, Errors and Failures in Real Systems, I/O performance measures, A little Queuing theory.

TEXTBOOKS

1. John L. Hennessey and David A. Patterson. *Computer Architecture: A Quantitative Approach, 5E*, Morgan-Kaufmann, 2012. ISBN-13: 978-0123838728.